Listing of Claims:

1. (currently amended) An integrated circuit comprising:

a two-dimensional pyramid filter architecture of an order 2N-1, where N is a positive integer greater than three, the two-dimensional pyramid filter architecture of an order 2N-1 including one-dimensional pyramid filters of order 2N-1 and summer circuits;

said two dimensional pyramid filter architecture of order 2N-1, in operation, capable of producing, on respective clock cycles, at least the following:

two pyramid filtered output signals corresponding to the summation by first and second summer circuits of the output signals produced by ten one-dimensional pyramid filters of order 2N-1; and

a pyramid filtered output ~~signals~~ signal corresponding to an output ~~signals~~ signal produced ~~either~~ by ~~four two-dimensional pyramid filters or one two-dimensional pyramid filter of order [2(N-1) – 1] using~~ summing signal sample matrices of order [2(N-1)-1] in a third summer circuit;

wherein the respective pyramid filtered output signals in said two dimensional pyramid filter architecture are summed by a fourth summer circuit on respective clock cycles of said two dimensional pyramid filter architecture.

2. (currently amended) The integrated circuit of claim 1, wherein N is five; and

wherein said two dimensional pyramid filter architecture of order nine, in operation, capable of producing, on respective clock cycles, the pyramid filtered output signals corresponding to the summation of ~~output signals produced either by four two-dimensional pyramid filters or one two-dimensional pyramid of order seven using~~ four signal sample matrices $P_{i-1,j-1}^{7x7}, P_{i-1,j+1}^{7x7}, P_{i+1,j-1}^{7x7}, P_{i+1,j+1}^{7x7}$ ~~, the pyramid filtered output signals being produced by a plurality of one-dimensional pyramid filters~~.

3. (currently amended) The integrated circuit of claim [[2]] 1, wherein said one-dimensional pyramid filters comprise a sequence of scalable cascaded ~~multiplerless~~ multiplierless operational units, each of said operational units capable of producing a different order pyramid filtered output signal sample stream.

4. (currently amended) The integrated circuit of claim [[2]] 1, wherein said one-dimensional pyramid filters comprise other than one-dimensional multiplierless pyramid filters.

5. (currently amended) The integrated circuit of claim [[2]] 1, wherein said [[~~two dimensional pyramid filter architecture of order nine, in operation, capable of producing, on respective clock cycles, the pyramid filtered output signals corresponding to output signals produced either by four two-dimensional pyramid filters or one two-dimensional pyramid of order seven using four signal sample matrices~~ $P^{7x7}_{i-1,j-1}, P^{7x7}_{i-1,j+1}, P^{7x7}_{i+1,j-1}, P^{7x7}_{i+1,j+1}$ ~~, the pyramid filtered~~]] output signals produced by a plurality of one-dimensional pyramid filters being produced by eight one-dimensional pyramid filters of order seven.

6. (original) The integrated circuit of claim 5, wherein, of the eight one-dimensional pyramid filters of order seven, four are applied row-wise and four are applied column-wise.

7. (currently amended) The integrated circuit of claim 5, wherein ~~said two dimensional pyramid filter architecture of order nine, in operation, capable of producing, on respective clock cycles, the pyramid filtered output signals corresponding to output signals produced by four two-dimensional pyramid filters of order seven, the pyramid filtered output signals produced by a plurality of one-dimensional pyramid filters being produced by~~ the eight one-dimensional pyramid filters of order seven comprise eight one-dimensional multiplierless pyramid filters of order seven.

8. (currently amended) The integrated circuit of claim 7, wherein, of the eight one-dimensional multiplierless pyramid filters of order seven, four are applied row-wise and four are applied column-wise.

9. (cancelled)

10. (cancelled)

11. (cancelled)

12. (currently amended) A method of filtering an image using a two-dimensional pyramid filter architecture of order 2N-1, where N is a positive integer greater than four, the two-dimensional pyramid filter architecture of order 2N-1 including one-dimensional pyramid filters of order 2N-1, said method comprising:

summing, on respective clock cycles of said two dimensional pyramid filter architecture, the following:

pyramid filtered output signals corresponding to output signals produced by ten one-dimensional pyramid filters of order 2N-1; and

pyramid filtered output signals corresponding to ~~output signals produced either by four two-dimensional pyramid filters or one two-dimensional pyramid filter of order [2(N-1) – 1] using~~ the summation of signal sample matrices of order [2(N-1)-1].

13. (cancelled)

14. (currently amended) The method of claim 12, wherein N is five; and

wherein the ~~pyramid filtered output signals corresponding to output signals produced either by four two-dimensional pyramid filters or one two-dimensional pyramid filter of order seven using~~ signal sample matrices comprise four signal sample matrices $P_{i-1,j-1}^{7x7}, P_{i-1,j+1}^{7x7}, P_{i+1,j-1}^{7x7}, P_{i+1,j+1}^{7x7}$ ~~comprise pyramid filtered output signals produced by a plurality of one-dimensional pyramid filters~~.

15. (currently amended) The method of claim [[14]] 12, wherein said one-dimensional pyramid filters comprise a sequence of scalable cascaded ~~multiplierless~~ multiplierless operational units, each of said operational units capable of producing a different order pyramid filtered output signal sample stream.

16. (currently amended) An article comprising: a storage medium, said storage medium having stored thereon instructions, that, when executed result in filtering an image using a two-dimensional pyramid filter architecture of order 2N-1, the two-dimensional pyramid filter architecture of order 2N-1 including one-dimensional pyramid filters of order 2N-1, where N is a positive integer greater than four, by:

summing, on respective clock cycles of said two dimensional pyramid filter architecture, the following:

pyramid filtered output signals corresponding to output signals produced by ten one-dimensional pyramid filters of order 2N-1; and

pyramid filtered output signals corresponding to ~~output signals produced either by four two-dimensional pyramid filters or one two-dimensional pyramid filter of order [2(N-1) – 1] using~~ the summation of signal sample matrices of order [2(N-1)-1].

17. (cancelled)

18. (currently amended) The article of claim 16, wherein N is five; and

wherein the ~~pyramid filtered output signals corresponding to output signals produced either by four two-dimensional pyramid filters or one two-dimensional pyramid of order seven using~~ signal sample matrices comprise four signal sample matrices $P^{7x7}_{i-1,j-1}, P^{7x7}_{i-1,j+1}, P^{7x7}_{i+1,j-1}, P^{7x7}_{i+1,j+1}$ ~~, comprise pyramid filtered output signals produced by a plurality of one-dimensional pyramid filters~~.

19. (currently amended) The article of claim [[18]] 16, wherein said one-dimensional pyramid filters comprise a sequence of scalable cascaded multiplierless operational units, each of said operational units capable of producing a different order pyramid filtered output signal sample stream.

20. (currently amended) An image processing system comprising:

an image processing unit to filter scanned color images;

said image processing unit including at least one two-dimensional pyramid filter architecture;

said at least one two-dimensional pyramid filter architecture comprising:

a two-dimensional pyramid filter architecture of an order 2N-1, where N is a positive integer greater than four, the two-dimensional pyramid filter architecture of order 2N-1 including one-dimensional pyramid filters of order 2N-1 and summer circuits;

said two dimensional pyramid filter architecture of order 2N-1, in operation, capable of producing, on respective clock cycles, at least the following:

two pyramid filtered output signals corresponding to the summation by first and second summer circuits of the output signals produced by ten one-dimensional pyramid filters of order 2N-1; and

a pyramid filtered output ~~signals~~ signal corresponding to an output ~~signals~~ signal produced ~~either~~ by ~~four two-dimensional pyramid filters or one two-dimensional pyramid filter of order [2(N-1) – 1] using~~ summing signal sample matrices of order [2(N-1)-1] in a third summer circuit;

wherein the respective pyramid filtered output signals in said two dimensional pyramid filter architecture are summed by a fourth summer circuit on respective clock cycles of said two dimensional pyramid filter architecture.

21. (cancelled)

22. (currently amended) The system of claim 20, wherein N is five; and

wherein the ~~pyramid filtered output signals corresponding to output signals produced either by four two-dimensional pyramid filters or one two-dimensional pyramid of order seven using~~ the signal sample matrices comprise four signal sample matrices $P_{i-1,j-1}^{7x7}, P_{i-1,j+1}^{7x7}, P_{i+1,j-1}^{7x7}, P_{i+1,j+1}^{7x7}$ ~~, comprise pyramid filtered output signals produced by a plurality of one-dimensional pyramid filters~~.

23. (currently amended) The system of claim [[22]] 20, wherein said one-dimensional pyramid filters comprise a sequence of scalable cascaded ~~multiplierless~~ multiplierless operational units, each of said operational units capable of producing a different order pyramid filtered output signal sample stream.